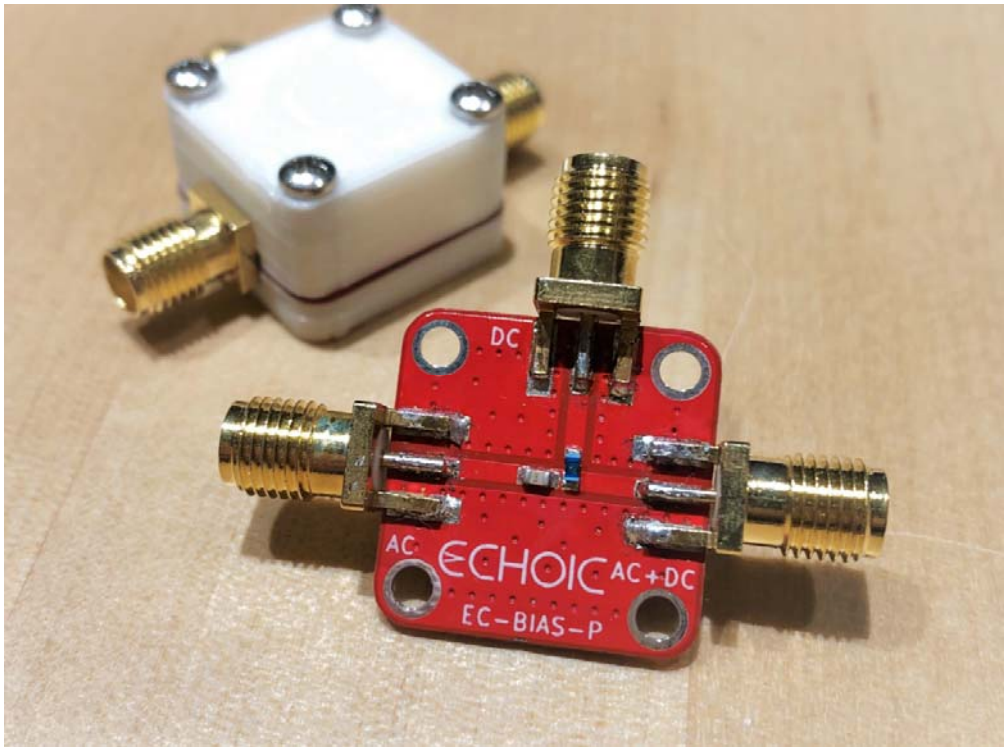
Data Sheet

EC-BIAS-P High Power Pulsed Bias Network 600MHz to 5GHz



Applications

- RF transistor characterization
- Power amplifiers
- Broadband amplifiers

Features

- Max VDC = 200V, Max IDC = 1A
- Return Loss and Isolation > 20dB over 700MHz BW
- Insertion loss < 1dB over 4.4 GHz BW

Description

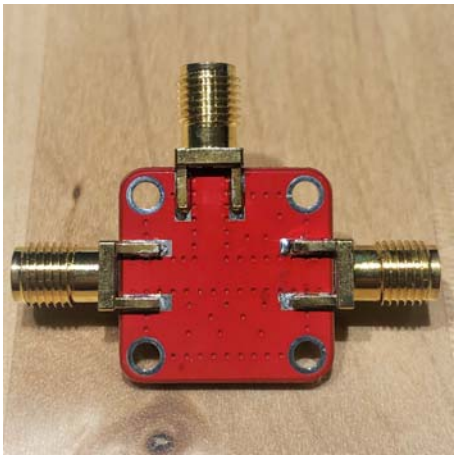
The EC-BIAS-P is a high performance bias tee network for pulsed bias applications. This pulsed bias network can be used for transistor characterization test and measurement as well as for pulsed amplifier development. The pulsed bias network has three ports: RF, DC and RF+DC. The RF port passes RF ("AC"), the DC port is used to feed DC, and the RF+DC ("AC+DC") port presents the combined signal to the device. The EC-BIAS-P can handle DC voltages up to 200V and DC currents up to 1A. Therefore, it is suitable for biasing high power transistor devices like GaN HEMTs. The EC-BIAS-P can also be used for static DC biasing.

The EC-BIAS-P's RF-to-RF+DC path operates from 600MHz to 5GHz when considering a maximum insertion loss of 1dB and minimum return loss of 10dB. The DC-to-RF and DC-to-RF+DC isolation is > 10dB from 0.817 GHz to 5.0GHz.

The EC-BIAS-P has excellent DC-to-RF+DC pulse performance exhibiting minimal pulse distortion from pulses with as low as 7 ns rise time. The pulse propagation delay from DC-to-RF+DC is 1.2ns. The EC-BIAS-P also exhibits minimal distortion for pulsed RF inputs.

Front side of EC-BIAS-P

Back side of EC-BIAS-P



Specifications

Parameter	*Test Cond.*	*Min.*	*Typ.*	*Max.*	*Units*
Impedance			50		Ohm
Operating Frequency	IL < 1dB	0.60		5.0	GHz
VSWR	0.6 to 5 GHz	1.007	1.25	1.8	
Return Loss	0.05 to 5 GHz			10	dB
	0.711 to 3.925			20	dB
Insertion loss	0.6 to 5 GHz	0.188	0.3	1.00	dB
Isolation	0.817 to 5 GHz	10			dB
	1.888 to 5 GHz	20			dB
Pulse prop. delay	DC to RF+DC port		1.2		ns
DC port voltage				200*	VDC/Vpulsed
DC port current				1*	ADC

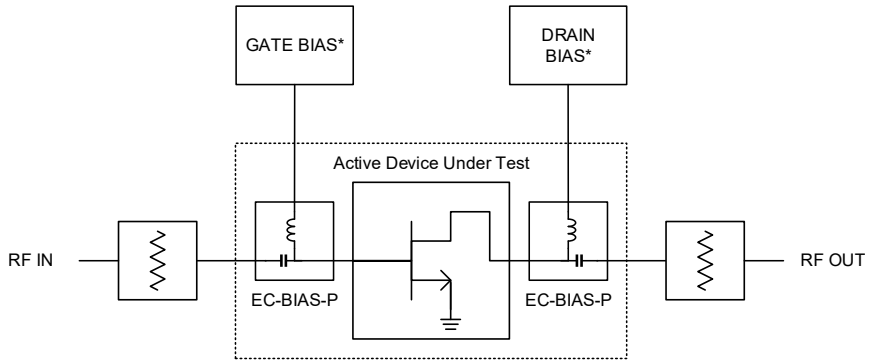
*based on component specs

Typical Application

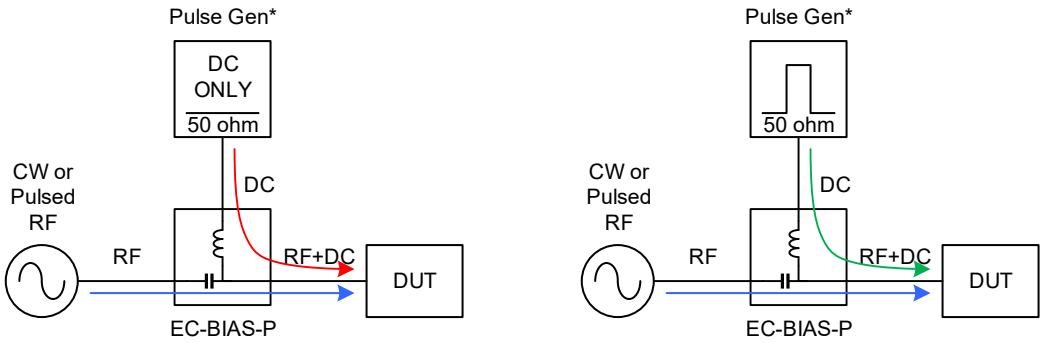
The EC-BIAS-P is typically used in conjunction with an active transistor device or amplifier requiring a DC bias at the device terminals. A conventional application with a transistor test fixture is shown below. In the diagram, one EC-BIAS-P is placed at the gate of the device and one is placed at the drain of the device. The input bias tee module receives an RF signal from a source, combines this with the bias voltage and applies the composite signal to the device gate. The gate voltage can be positive or negative, making it suitable for all FET devices. The output bias tee simultaneously feeds the bias voltage to the drain and allows for the RF output produced by the transistor to pass to the next stage.

The EC-BIAS-P can be driven in a number of ways. The DC input can consist of either a pulsed DC or static DC voltage. The RF input can consist of a pulsed RF or a CW RF signal. Several combinations of the pulsed/static DC and pulsed/CW RF can be used to excite an active device as shown below.

Pulsed/CW transistor characterization setup using EC-BIAS-P



Various ways to drive a device under test (DUT such as a transistor terminal) using the EC-BIAS-P



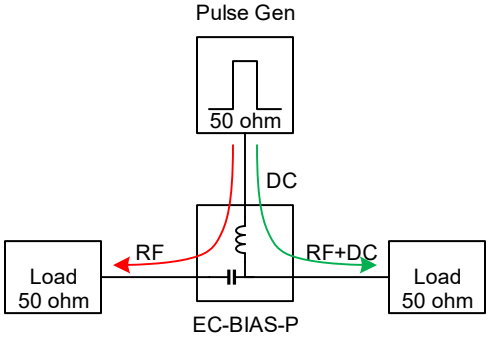
***For FET devices, it is highly recommended that a pulse generator be used for the Gate Bias *in both pulsed and static DC operation to ensure stability*. The pulse generator's 50 ohm source impedance will present a low frequency termination to the DUT. This is less critical at the Drain Bias, but is still recommended if available. Use the DC offset function on your pulse generator to provide this static DC bias.**

Performance

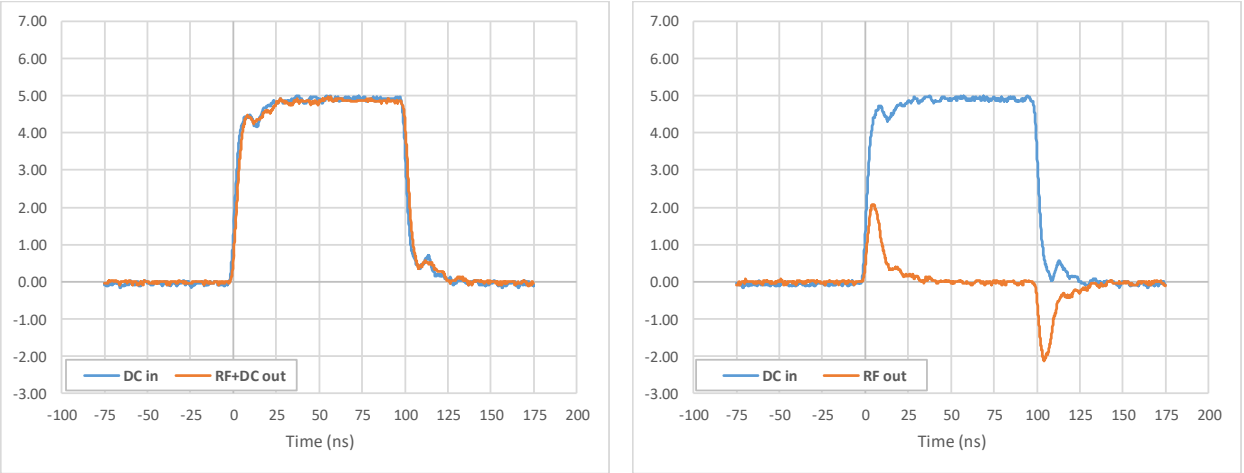
Pulsed DC Performance

The pulsed DC test setup of the EC-BIAS-P is shown below. In this characterization setup, the EC-BIAS-P is excited with a DC pulse at the DC input port. Both the RF and RF+DC ports are terminated with 50 ohm loads. The performance of the pulse can be evaluated by measuring the response at the loaded RF and RF+DC ports.

EC-BIAS-P pulsed DC bias test setup

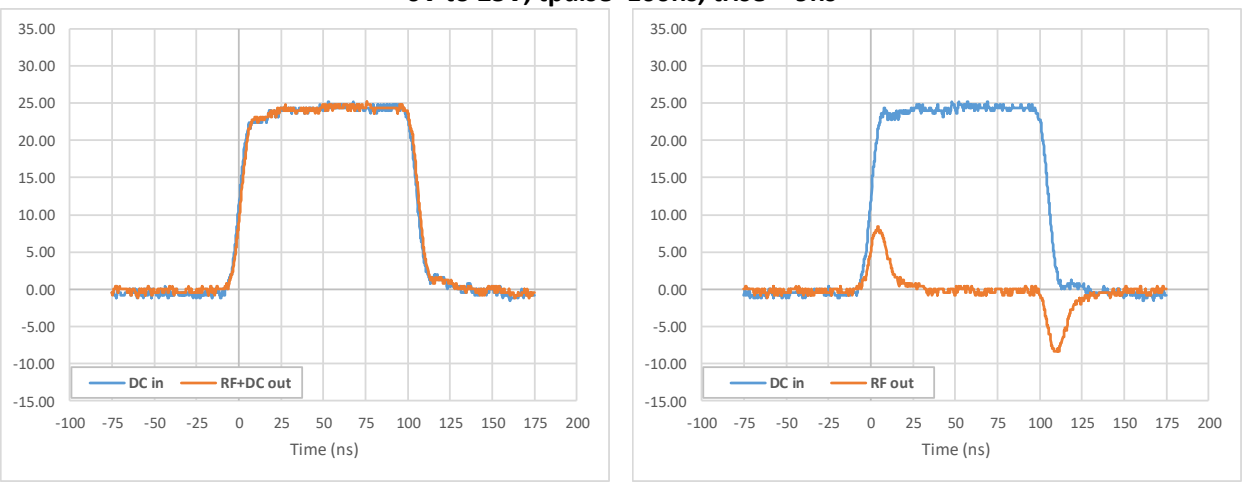


0V to 5V, tpulse=100ns, trise=~7ns



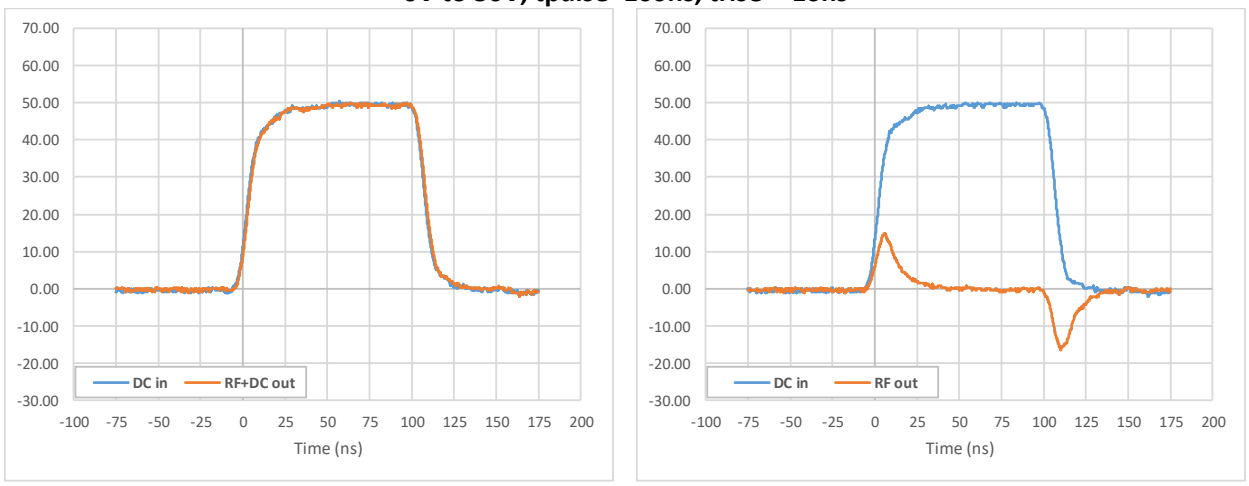
For a 100ns 5V pulse, the EC-BIAS-P shows little to no distortion as the pulse travels from the DC to the RF+DC path (left). Due to the fast risetime of 7ns, some of the pulse energy during that transition is passed from the DC to the RF port (right). Therefore, care should be takes to increase the pulse rise/fall time or to use an attenuator if the RF port if used as an input. This is to limit the pulse energy feeding back to the RF source.

0V to 25V, tpulse=100ns, trise=~9ns



For a 100ns 25V pulse, the EC-BIAS-P shows little to no distortion as the pulse travels from the DC to the RF+DC path (left). Similar to the previous case, a fast risetime of 9ns causes some of the pulse energy to pass from the DC to the RF port (right). Therefore, care should be takes to increase the pulse rise/fall time or to use an attenuator if the RF port if used as an input. This is to limit the pulse energy feeding back to the RF source.

0V to 50V, tpulse=100ns, trise=~16ns

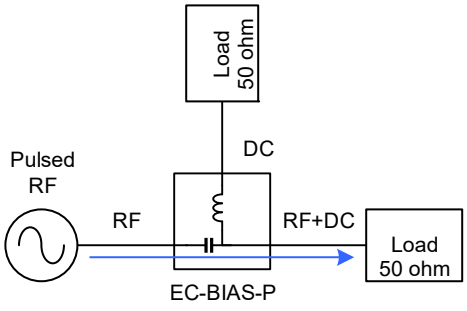


In this third example, for a 100ns 50V pulse, the EC-BIAS-P again shows little to no distortion as the pulse travels from the DC to the RF+DC path (left). Similar to the previous case, the risetime of 16ns causes some of the pulse energy to pass from the DC to the RF port (right). If RF is used as an input, an increased the pulse rise/fall time or an attenuator at the RF port should be used. This is to limit the pulse energy feeding back to the RF source.

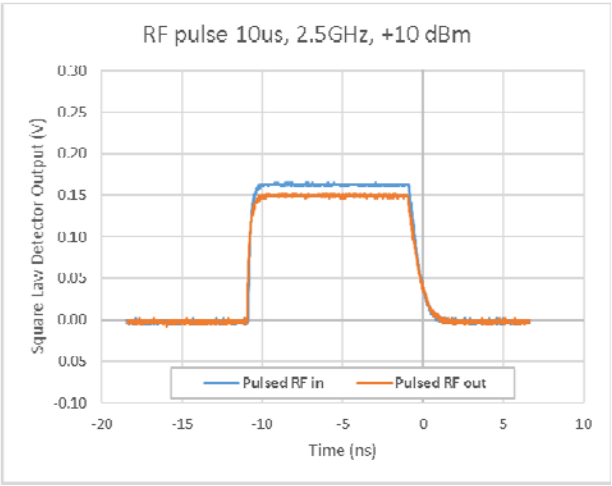
Pulsed RF Performance

In this pulsed RF example, the RF port is excited with a 10us, 2.5GHz, +10dBm RF pulse and the time-domain RF power pulse is measured using a square law detector. The detector is used to record the RF pulse available from the source and then used to record the RF pulse which passes through the RF to RF+DC path of the EC-BIAS-P board. The DC port is terminated in 50 ohms. The EC-BIAS-P exhibits no distortion of the RF pulse and passes on average 93.83% (0.152V / 0.162V = 0.9383) of the incident RF pulse power equivalent to a -0.2765 dB gain at 2.5GHz.

EC-BIAS-P pulsed RF test setup



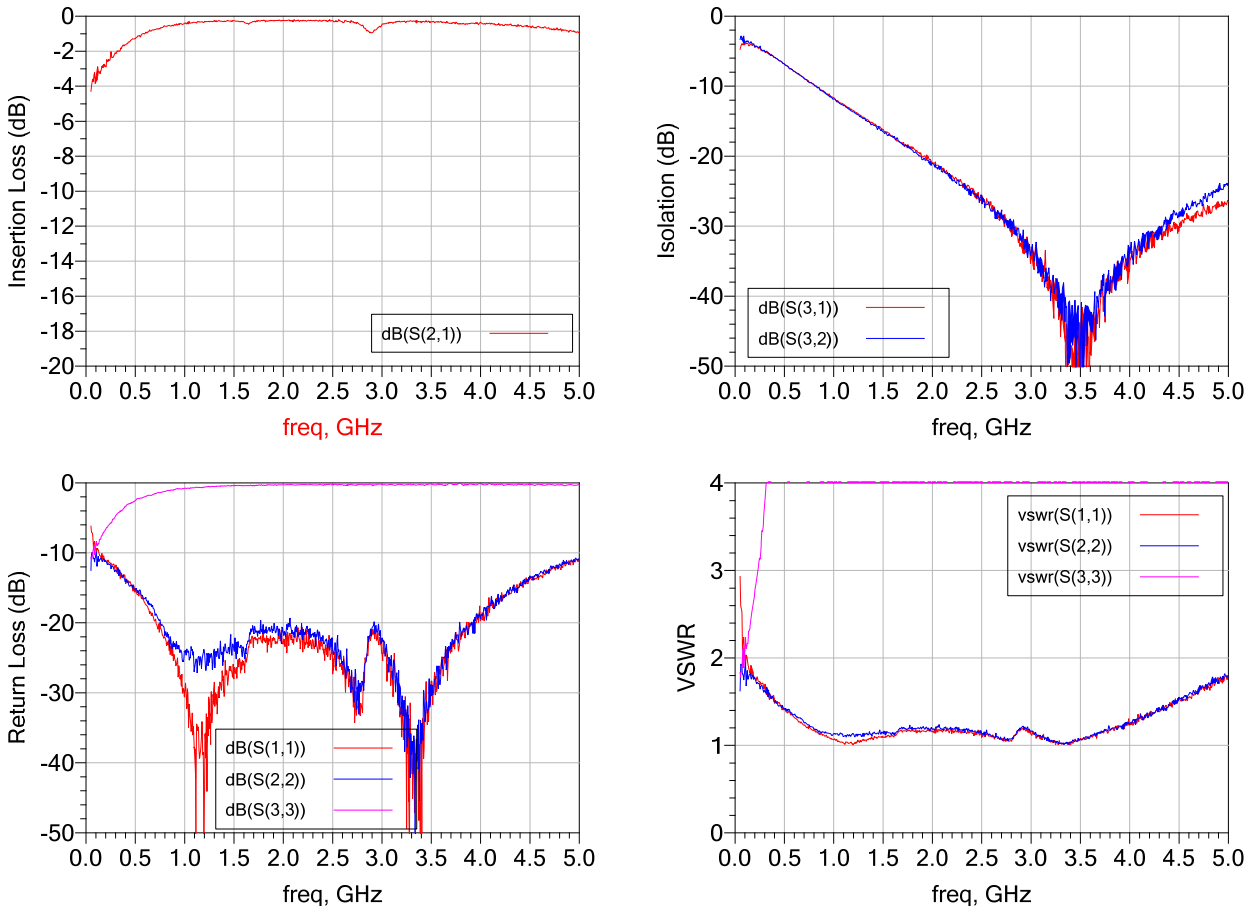
EC-BIAS-P pulsed RF test measurements



Small-signal Performance

The S-parameters for the EC-BIAS-P are provided below. The three port network consisting of RF (port 1), RF+DC (port 2), DC (port 3) ports are measured from 0.05 GHz to 5.0 GHz and show excellent insertion loss, return loss and isolation.

Typical S-parameters from 0.05 to 5.0 GHz

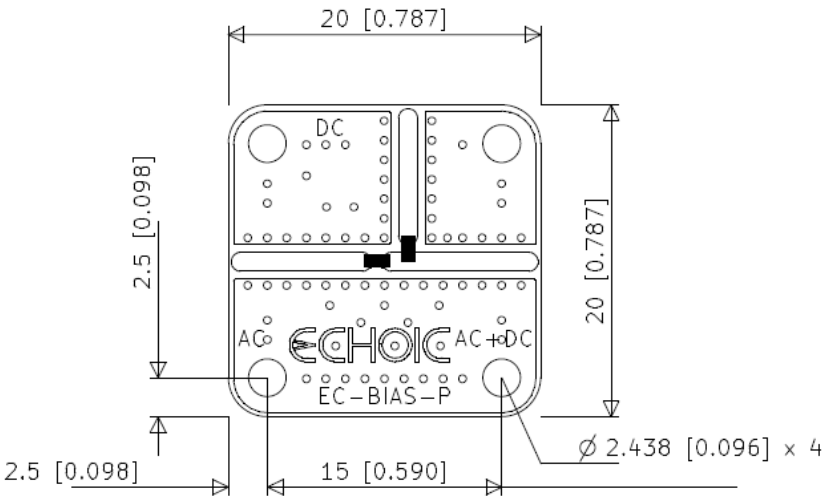


Mechanical

PCB mechanical drawing. All units in mm [inches]. Connectors not shown.

Configuration	*Parameter*	*Typical*	*Units*
PCB only	Width	20	mm
(w/o case, w/o connectors)	Length	20	mm
	Height	0.82	mm
PCB and case	Width	20.15	mm
(w/o connectors)	Length	20.15	mm
	Height	13.28	mm
Connector	Torque	8	In-lbs

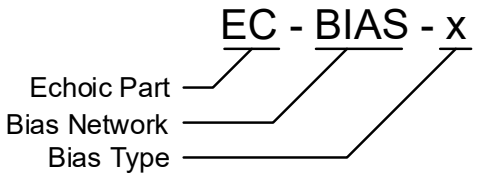
PCB mechanical drawing. All units in mm [inches]. Connectors not shown.



The EC-BIAS-P can be used with the optional case.

Ordering Information

Please use the following model number designation for ordering this and any other part from our bias line:



For example, EC-BIAS-P is an Echoic part, bias network for pulsed operation.

Web Resource

For more information on other industrial RF and microwave solutions please visit our online store 5G Links: www.5glinks.com